REMARKS

Favorable reconsideration of the application is respectfully requested in light of the amendments and remarks herein.

Upon entry of this amendment, claims 7-26 will be pending. By this amendment, claims 7, 10, 11, 14, 15, 18, 19, and 22 have been amended. No new matter has been added.

§102 Rejection of Claims 7-26

In Section 2 of the Office Action, the Examiner has rejected claims 7-26 under 35 U.S.C. §102(e) as being anticipated by Niijima *et al.* (U.S. Patent No. 5,889,795; hereinafter referred to as "Niijima").

In the Background section of the Specification, it was disclosed that "in case of the flash memory of 4 MB (megabytes), as shown in Fig. 12, one segment is divided into 512 clusters. The segment is a unit for managing a predetermined number of clusters. One cluster is divided into 16 sectors. One cluster has a capacity of 8 kB (kbytes). One sector has a capacity of 512 B. A memory of a capacity of 16 MB can be constructed by using four segments each having a capacity of 4 MB." *Background of the Specification, page 2, lines 17-25.* It was further disclosed that "[a] physical address is added to each cluster in the flash memory. A correspondence relation between the clusters and the physical addresses is unchanged." *Background of the Specification, page 3, lines 7-10.*

Thus, "for a data construction of one sector on the flash memory, as shown in Fig. 18, an area having a length of 16 bytes in which management information is recorded is added to data of 512 bytes. The management information comprises a logic cluster number, cluster

management information, and attribute information." *Background of the Specification, page 7, lines 12-18.*

"In the conventional switching of the storages of the flash memory mentioned above, a storage selection signal is formed by using a few bits from the MSB of the address. Thus, the segments are concentratedly arranged onto one storage and the segments are different every storage. According to such a method, a plurality of clusters of the same segment cannot be simultaneously written in parallel." *Background of the Specification, page 9, lines 15-23.*

Therefore, it can be seen that the logical/physical address correspondence in terms of the distribution of clusters into a plurality of storages can cause problems in the conventional flash memory.

To solve the above-described problems, embodiments of the present invention provide system and method for recording data on a memory. For example, the structure of claim 7, as presented herein, includes:

"a plurality N of nonvolatile storages, each storage including at least one cluster of data recorded, where each cluster is constructed by a plurality K of sectors;

address designating means for designating an address of the cluster in which data is recorded; and

recording means for recording data into a storage location at the address designated by said address designated means,

wherein said plurality N of nonvolatile storages is divided into a plurality of segments, each segment distributed and arranged into said plurality of storages, said each segment composed of a plurality of clusters, where *each cluster of first N clusters of said each segment configured to consecutively store first to Kth entire sectors in first to Kth memory locations,*

respectively, of a corresponding one of said plurality N of nonvolatile storages, such that said first N clusters of each segment are continuously arranged across said N storages." (emphasis added)

Therefore, claim 7 describes, in one aspect, a configuration of a nonvolatile memory having N storages (*e.g.*, N=4 as shown in Fig. 11), where the first N clusters are arranged across the N storages as shown in Fig. 11. Further, each cluster includes K sectors (*e.g.*, K=16 as shown in Fig. 5), which are consecutively stored in first K memory locations of a corresponding one storage as shown in Fig. 5.

However, it can be seen in Figs. 5-10 of Niijima that sectors (referred to as sectors in Fig. 5 and Figs. 7-10 but referred to as Bn in Fig. 6) of each cluster are not stored consecutively in one storage. Unlike the description of the limitation in claim 7 (and as shown in Fig. 5 of the present application), Figs. 5-10 of Niijima indicate that consecutively-numbered sectors are stored in different storages such that a single cluster spans multiple storages.

It was indicated in the Background section that management information in one sector on the flash memory includes "a logic cluster number, cluster management information, and attribute information". However, since the memory in Niijima is configured such that the plurality of sectors within one cluster are distributed among multiple storages, Niijima's memory cannot address the problems of the conventional flash memory described above with respect to the logical/physical address correspondence in terms of the distribution of clusters into the plurality of storages. The nonvolatile memory as configured in claim 7 addresses the problems of the conventional flash memory.

Based on the foregoing discussion, it is submitted that claim 7 is not anticipated by the teachings of Niijima. Independent claims 11, 15, and 19 closely parallel, and include substantially similar limitations as, independent claim 7. Further, claims 8-10, 12-14, 16-18, 20-22, and 23-26 depend from claims 7, 11, 15, and 19. Accordingly, it is submitted that the Examiner's rejection of claims 7-26 based upon 35 U.S.C. §102(e) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

Conclusion

In view of the foregoing, entry of this amendment, and the allowance of this application, with claims 7-26 is respectfully solicited.

In regard to the claims amended herein and throughout the prosecution of this application, it is submitted that these claims, as originally presented, were patentably distinct over the prior art of record, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes that have been made to these claims were not made for the purpose of patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these changes were made simply for clarification and to round out the scope of protection to which Applicant is entitled.

In the event that additional cooperation in this case may be helpful to complete its prosecution, the Examiner is cordially invited to contact Applicant's representative at the telephone number written below.

The Commissioner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account 50-0320.

Respectfully submitted,

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